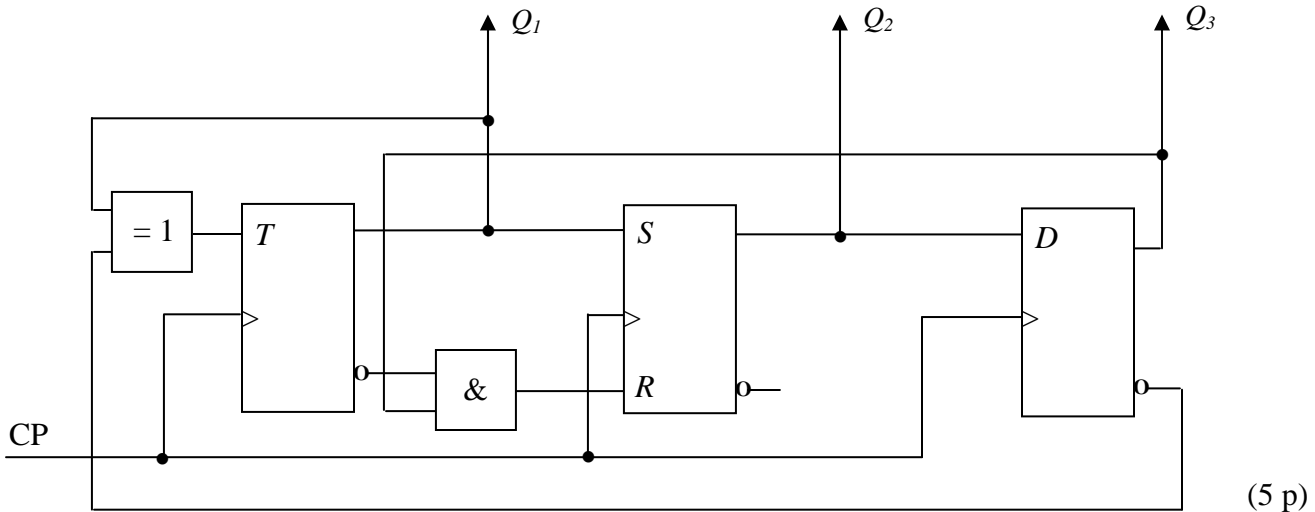


TMEL53 Digitalteknik – Dugga 3 – 15 februari 2013.

TMEL53 Switching Theory and Logical Design – Quiz 3 – 15th February 2013.

1. Beskriv funktionen hos sekvensnätet nedan genom att rita en tillståndsgraf.

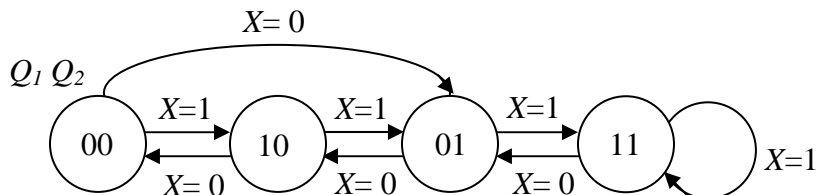
Describe the function of the sequential circuit below by drawing a state graph.



(5 p)

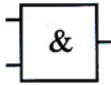
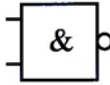
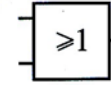
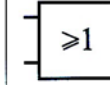
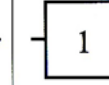

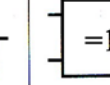




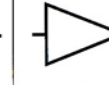
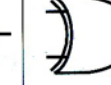

2. Konstruera ett sekvensnät som fungerar enligt tillståndsgrafens nedan. JK-vippor och valfria grindar får användas. För full poäng krävs att konstruktionen är minimal.

Realize a sequential circuit acting as shown in the state graph below. JK flip-flops and optional gates may be used. Full points require that the realization is as small as possible.



(5 p)

Tabeller över grindar

		$A \cdot B$	$\overline{A \cdot B}$	$A + B$	$\overline{A + B}$	\overline{A}	$A \oplus B$	$\overline{A \oplus B}$
A	B	AND	NAND	OR	NOR	INVERS	XOR	XNOR
0	0	0	1	0	1		0	1
0	1	0	1	1	0	1	1	0
1	0	0	1	1	0	0	1	0
1	1	1	0	1	0		0	1
IEC								
USA								

Tabeller över vippor

S	R	Q	J	K	Q	D	Q	T	Q
0	0	Q_0	0	0	Q_0	0	0	0	Q_0
0	1	0	0	1	0	1	1	1	$\overline{Q_0}$
1	0	1	1	0	1				
1	1		1	1	$\overline{Q_0}$				

Q	S	R	J	K	D	T	Q^+
0	0	-	0	-	0	0	0
0	1	0	1	-	1	1	1
1	0	1	-	1	0	1	0
1	-	0	-	0	1	0	1